

1 16. (AMENDED) The device of claim 15 wherein the embrittled region is  
2 created by an ion implantation.

1 17. (AMENDED) A device comprising:  
2 a silicon layer;  
3 a SiO<sub>2</sub> layer in contact with the silicon layer; and  
4 a strained silicon layer on top of the SiO<sub>2</sub> layer, the strained silicon layer being  
5 transferred from a wafer, the wafer having a stack structure of a base substrate and a layer  
6 of relaxed film.

1 18. (AMENDED) The device of claim 17 wherein the relaxed film is a relaxed  
2 SiGe layer.

1 19. (AMENDED) The device of claim 18 wherein the wafer further comprises  
2 an embrittled region.

1 20. (NEW) The device of claim 17 wherein the strained silicon layer is  
2 transferred to top of the SiO<sub>2</sub> layer by a bonded-etch back process.

1 21. (NEW) The device of claim 17 wherein the base substrate is a silicon layer.

1 22. (NEW) The device of claim 17 wherein the heat treatment uses a  
2 temperature range of approximately 400°C to 600°C.

1 23. (NEW) The device of claim 14 wherein the relaxed layer is a relaxed SiGe  
2 layer.

1 24. (NEW) The device of claim 23 wherein the relaxed SiGe layer has a  
2 thickness ranging from 0.1µm to 3.0µm.

1 25. (NEW) The device of claim 16 wherein the ion implantation uses an energy  
2 range of approximately 1keV to 20keV.

1           26.     (NEW) The device of claim 16 wherein the ion implantation uses a dose  
2 range of approximately  $1\text{E}16/\text{cm}^3$  to  $1\text{E}18/\text{cm}^3$ .

1           27.     (NEW) The device of claim 16 wherein the ion implantation uses hydrogen  
2 ions.

1           28.     (NEW) A wafer structure comprising:  
2           a first wafer having a first base substrate, a relaxed film layer, and a strained film  
3 layer; and  
4           a second wafer having a second base substrate and an oxidized film layer, the  
5 second wafer being bonded to the first wafer by a fire heat treatment, the strained film layer  
6 being transferred to the second wafer after the second wafer is separated from the first  
7 wafer by a second heat treatment.

1           29.     (NEW) The wafer structure of claim 28 wherein one of the first and second  
2 base substrates is a silicon layer.

1           30.     (NEW) The device of claim 28 wherein the relaxed film is a relaxed SiGe  
2 layer.

1           31.     (NEW) The device of claim 28 wherein the strained film layer is a strained  
2 silicon layer.

1           32.     (NEW) The device of claim 28 wherein the first heat treatment uses a  
2 temperature range of approximately  $100^\circ\text{C}$  to  $300^\circ\text{C}$ .

1           33.     (NEW) The device of claim 28 wherein the second heat treatment uses a  
2 temperature range of approximately  $400^\circ\text{C}$  to  $600^\circ\text{C}$ .